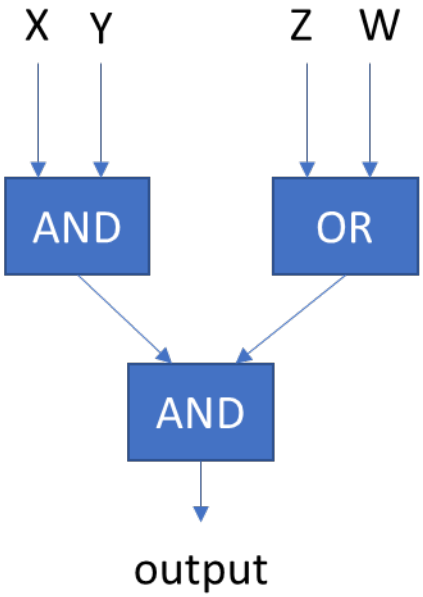
Exercise 3

1. **Logic gates**

What is the logic gate output of the following network given the input in the table below?



X	Y	Z	W	OUTPUT
ON	ON	ON	ON	
ON	ON	OFF	OFF	
OFF	ON	OFF	ON	
ON	ON	OFF	ON	

2. **Simulation of C1-FFL**

The model below describes a type I coherent feed-forward loop with an AND gate at the Z promoter. The AND gate is approximated by the product of the input of X (Sx) and the input of Y (activating hill function with hill coefficient n=2 and half-saturation constant k)

$$y'[t] == \mathrm{Sx} * \beta - \alpha * y[t]$$

$$z'[t] == \beta * \mathrm{Sx} * \frac{\left(\frac{y[t]}{k}\right)^2}{\left(1 + \left(\frac{y[t]}{k}\right)^2\right)} - \alpha * z[t]$$

a. Simulate dynamics of this model computational and show that there is a delay in the response of z upon on switch. Sx is the signal activating X, which can be 1 or 0. Assume for simplicity that all degradation and production rates are 1. Use k = 1.
b. Change k to values other than 1 and explain in words what you observe.
c. How do you have to change the model equations to represent a C1-FFL with positive autoregulation on y?

3. Non-monotonic input function

The following model describes an incoherent FFL

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y' == Sx*β - α*y
z' == Sx*β /(1+(y/k)^2) - α*z
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For mathematical simplicity, assume: β=1, α=1, k=1.

a. Plot z as a function of Sx from Sx = 0 to 10.

b. Calculate the activation signal Sx at which the steady-state of Z is maximal.

Hint: calculate steady-state of z as a function of S_x, then find the maximum of z with respect to S_x (where the first derivative of z with respect to S_x is zero: $dz/dS_x = 0$). You can do this by hand with pen and paper, or using algebraic functions of Mathematica, or any other tool you like.